

Dhaka International University

Lab Report details:

Lab Report Topic : Verification of Half Adder and Full Adder Circuit  
Lab Report No : 03  
Course Title : Digital Logic Design Lab  
Course Code : 713-204

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Date of Submission:14.5.25

**LAB REPORT**

**Title:** Verification of Half Adder and Full Adder Circuit

**Experiment No:** 3

**Objective**

To design, implement, and verify the truth tables and logic circuits of Half Adder and Full Adder using logic gates.

**1. Introduction**

Binary adders are fundamental components in digital electronics.

* A **Half Adder** adds two binary digits and outputs a **Sum** and a **Carry**.
* A **Full Adder** adds three binary digits (two inputs and a carry-in) and provides a **Sum** and **Carry-out**.

**2. Components Required**

* Logic Gate ICs (AND, OR, XOR)
* Breadboard and connecting wires
* Power supply (+5V)
* LED indicators

**3. Theory**

**Half Adder**

* **Inputs:** A, B
* **Outputs:** Sum (S), Carry (C)
* **Equations:**
  + Sum (S) = A ⊕ B
  + Carry (C) = A · B

**Truth Table:**

| **A** | **B** | **S (Sum)** | **C (Carry)** |
| --- | --- | --- | --- |
| 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |

**Full Adder**

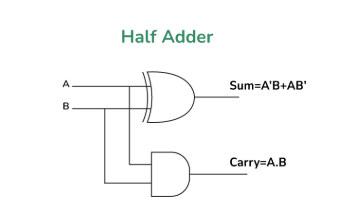
* **Inputs:** A, B, Cin (Carry-in)
* **Outputs:** Sum (S), Carry-out (Cout)
* **Equations:**
  + Sum (S) = A ⊕ B ⊕ Cin
  + Carry (Cout) = AB + BCin + ACin

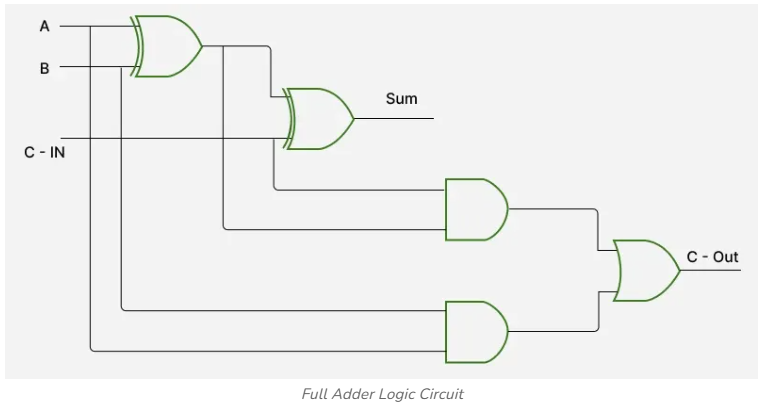
**Truth Table:**

| **A** | **B** | **Cin (Carry-in)** | **S (Sum)** | **Cout (Carry-out)** |
| --- | --- | --- | --- | --- |
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 | 0 |
| 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 1 | 0 | 1 |
| 1 | 0 | 0 | 1 | 0 |
| 1 | 0 | 1 | 0 | 1 |
| 1 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 1 |

**4. Circuit Diagrams**

* **Half Adder:**
  + XOR gate for **Sum**
  + AND gate for **Carry**
* **Full Adder:**
  + Two XOR gates for **Sum**
  + Three AND gates and two OR gates for **Carry**





**5. Procedure**

1. Connect the logic gates as per the circuit diagrams.
2. Apply binary combinations to inputs A and B (and Cin for Full Adder).
3. Observe and record outputs for **Sum** and **Carry**.
4. Verify the outputs against the theoretical truth tables.

**6. Observations**

The practical results of both Half Adder and Full Adder matched their respective truth tables. The logic gates functioned as expected.

**7. Conclusion**

The Half Adder and Full Adder circuits were successfully implemented and verified. The outputs aligned with theoretical predictions, validating the correctness of the digital logic circuits.